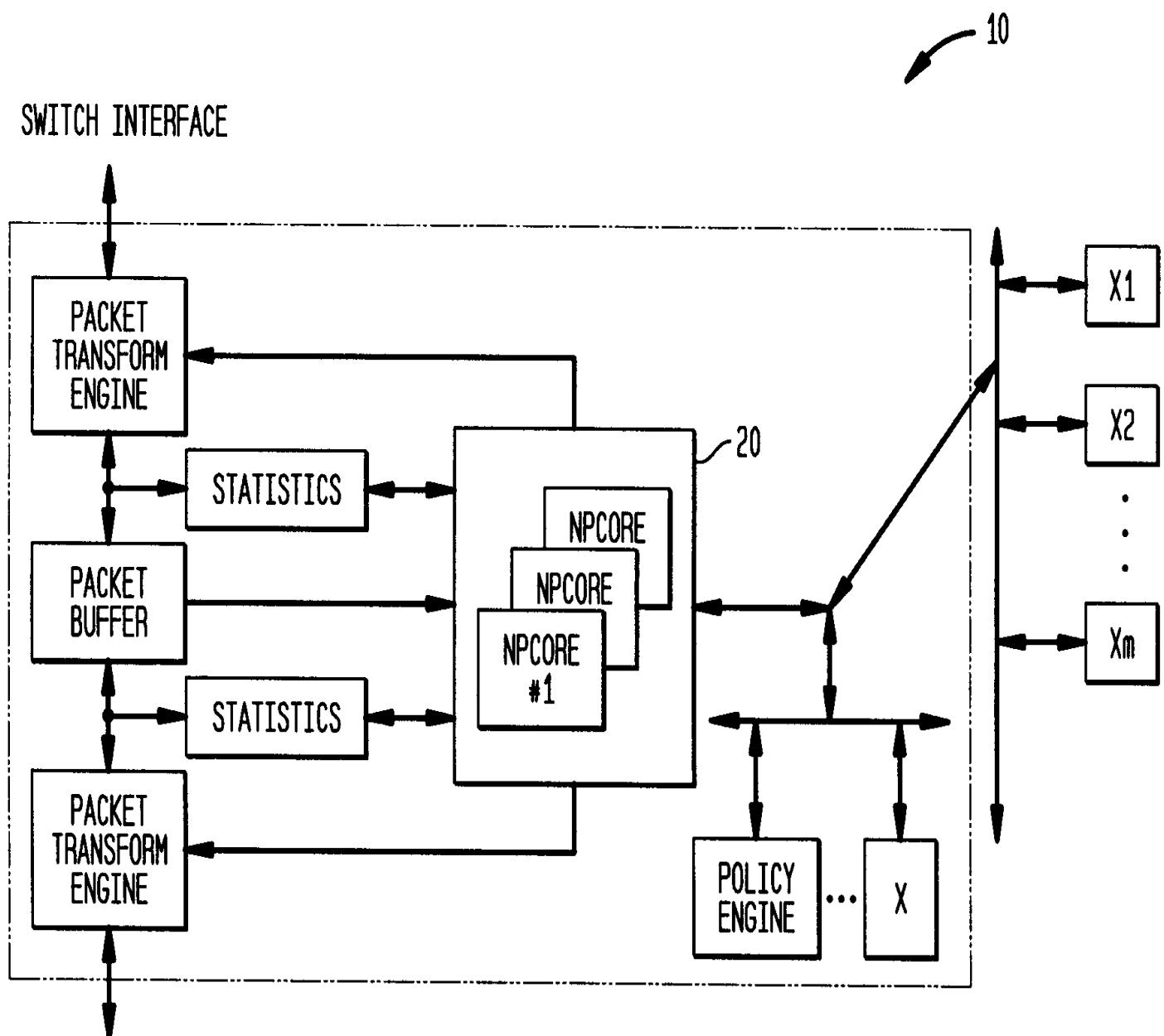


FIG. 1
(PRIOR ART)



MULTIPLE PHY INTERFACES

FIG. 2
(PRIOR ART)

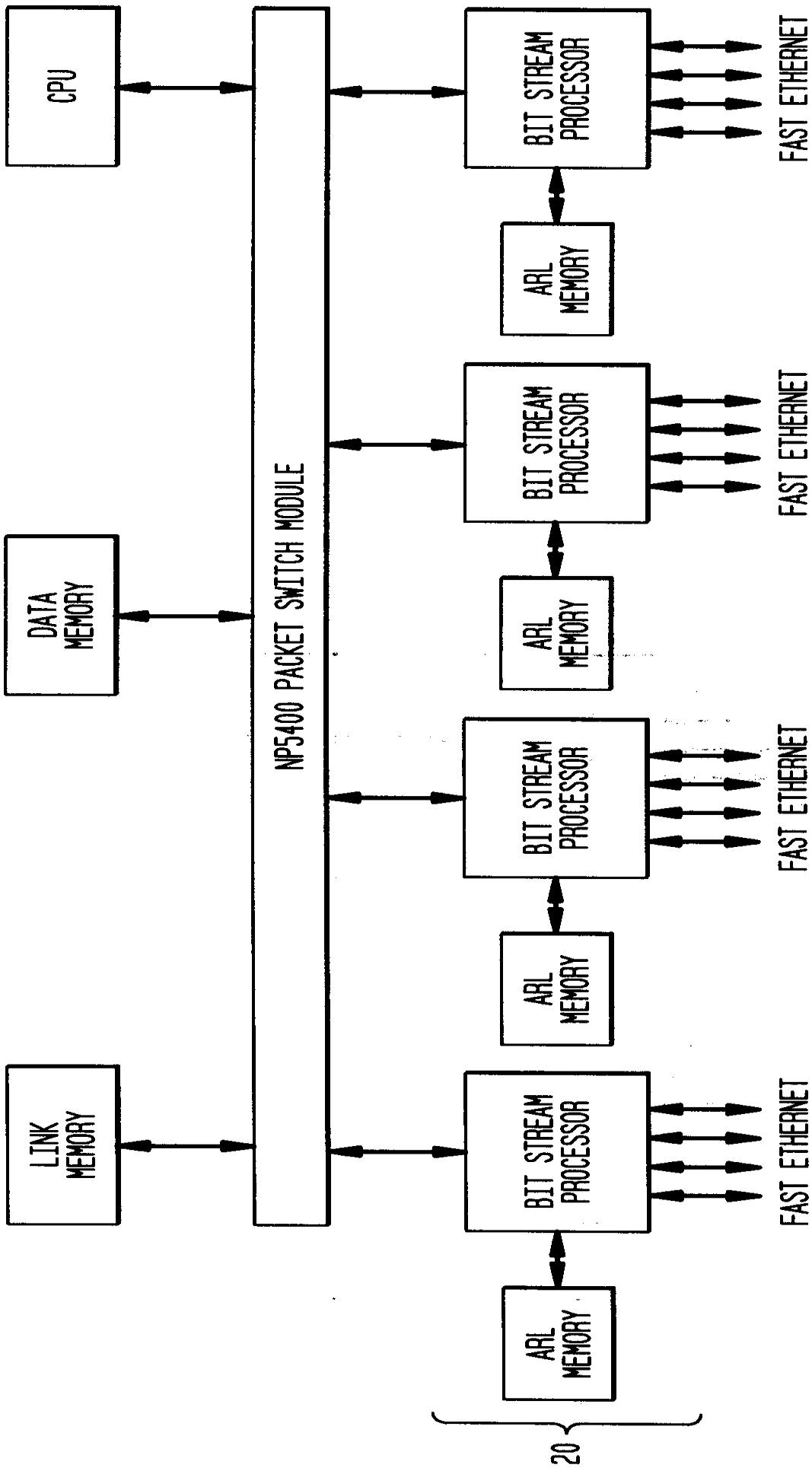


FIG. 3
(PRIOR ART)

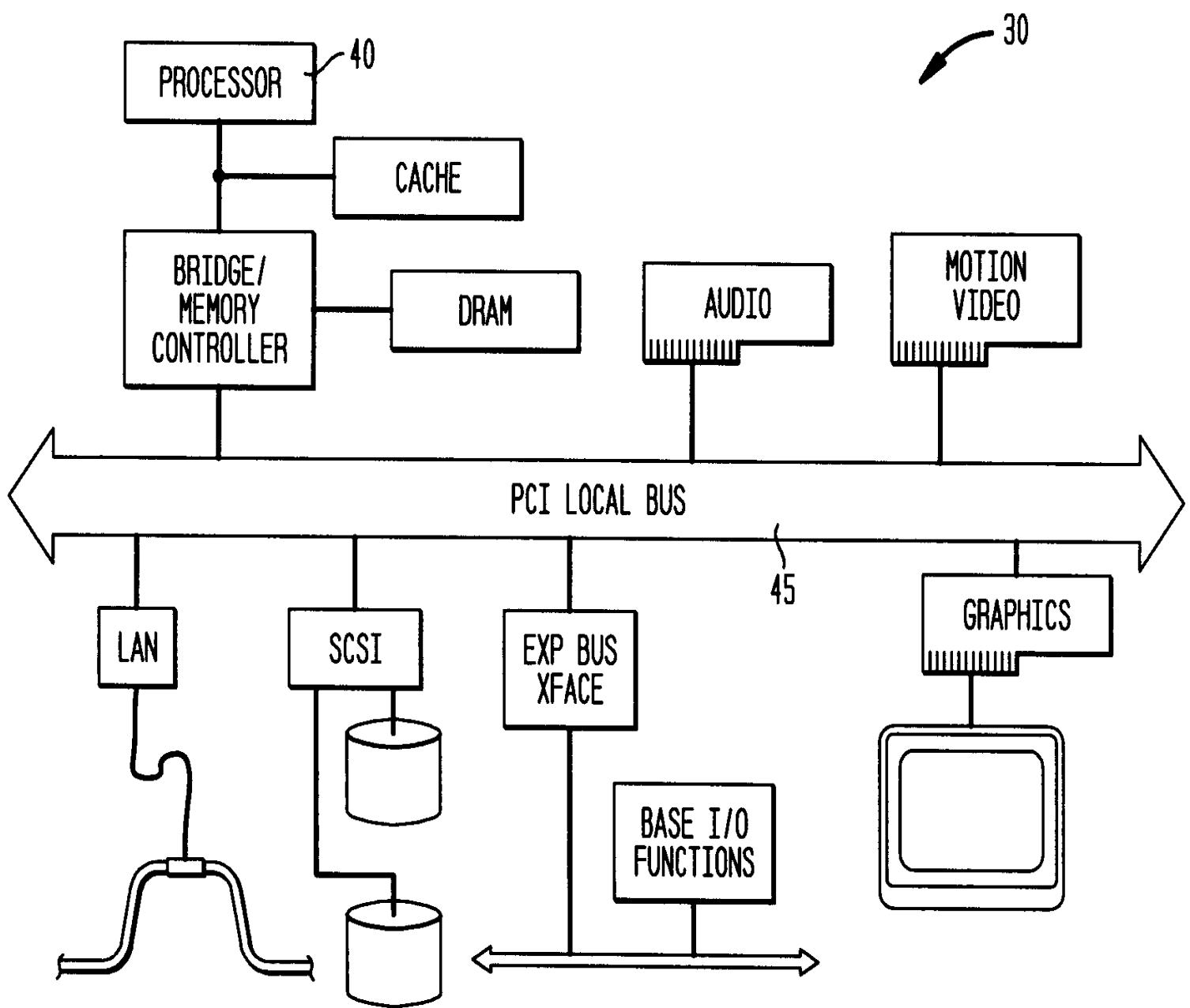


FIG. 4A

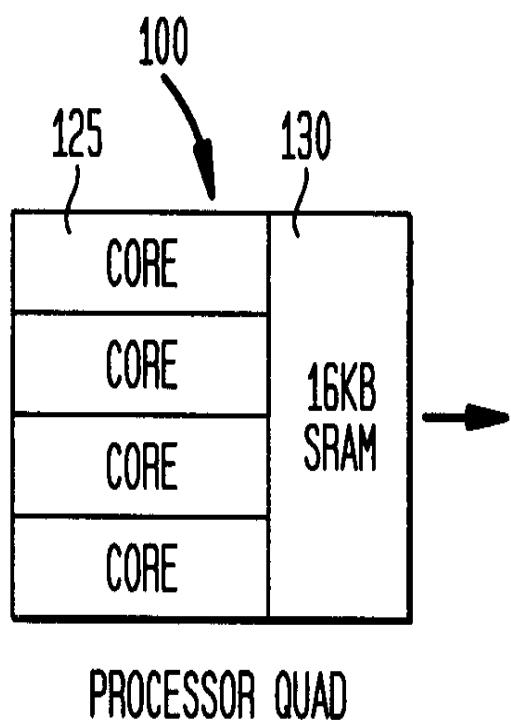
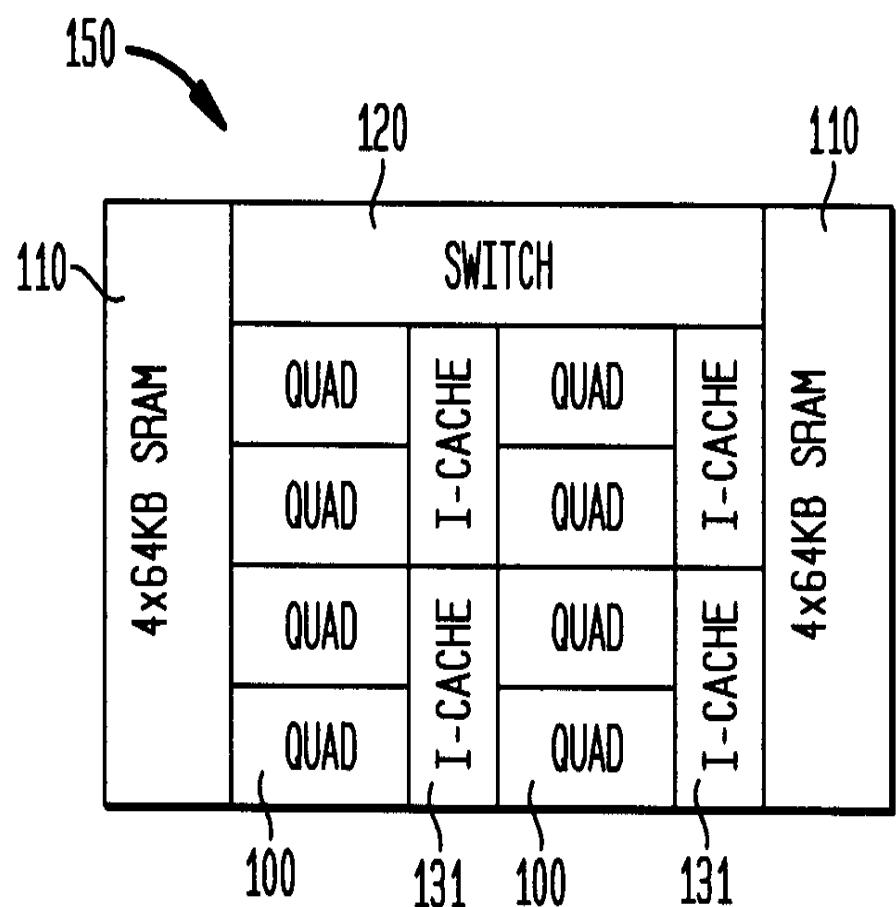


FIG. 4B



32-PROCESSOR SYSTEM

FIG. 5

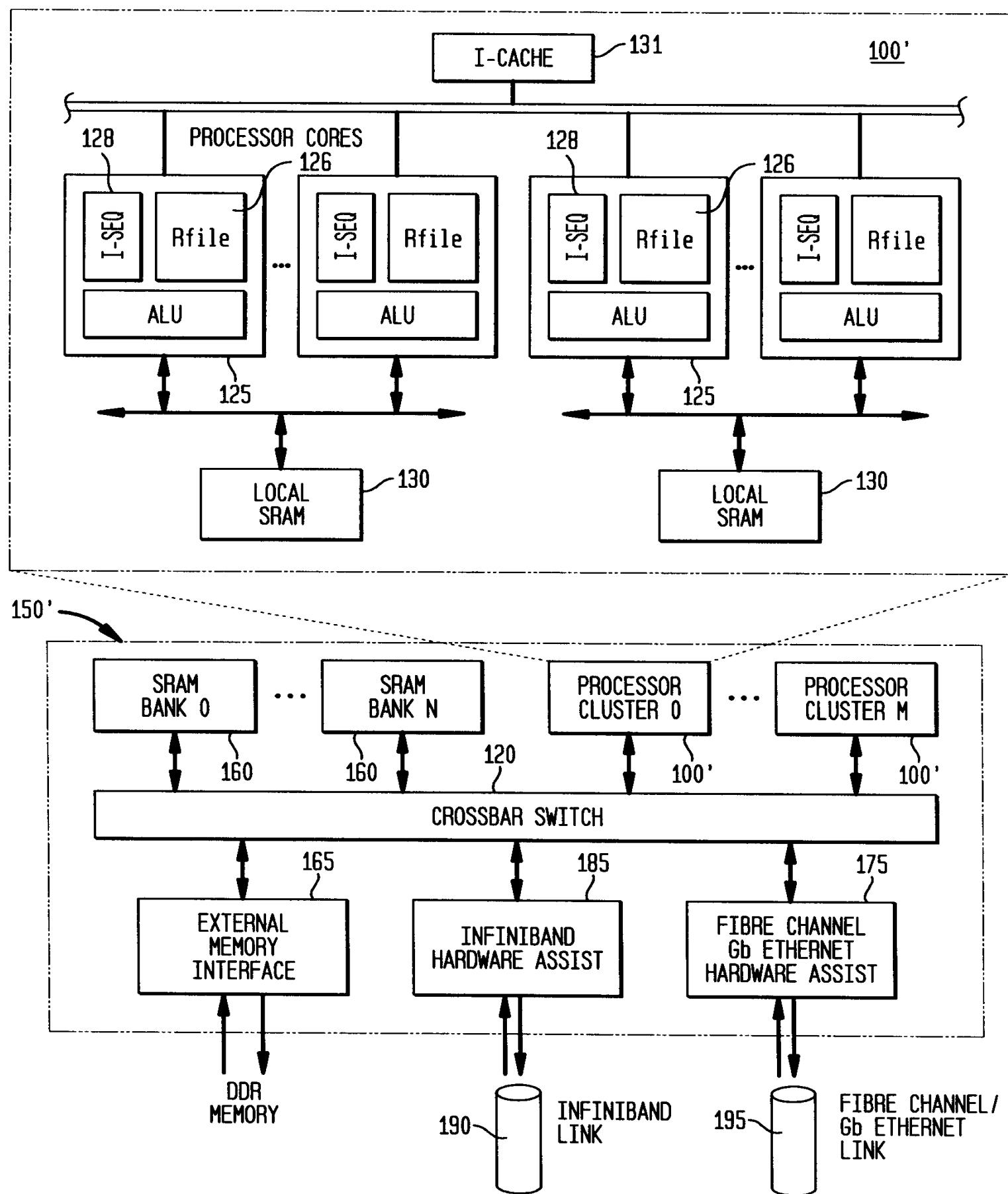


FIG. 6

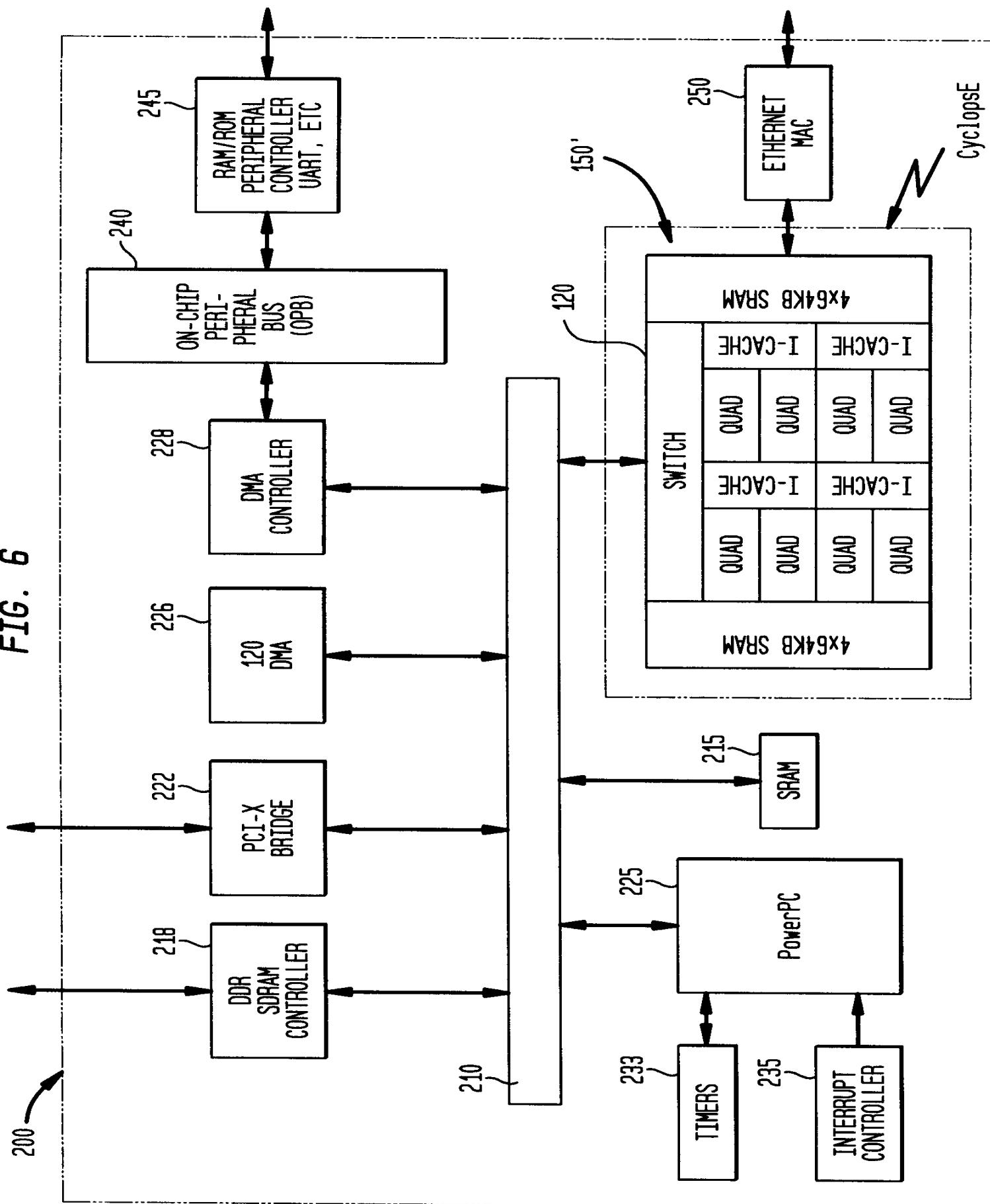


FIG. 7

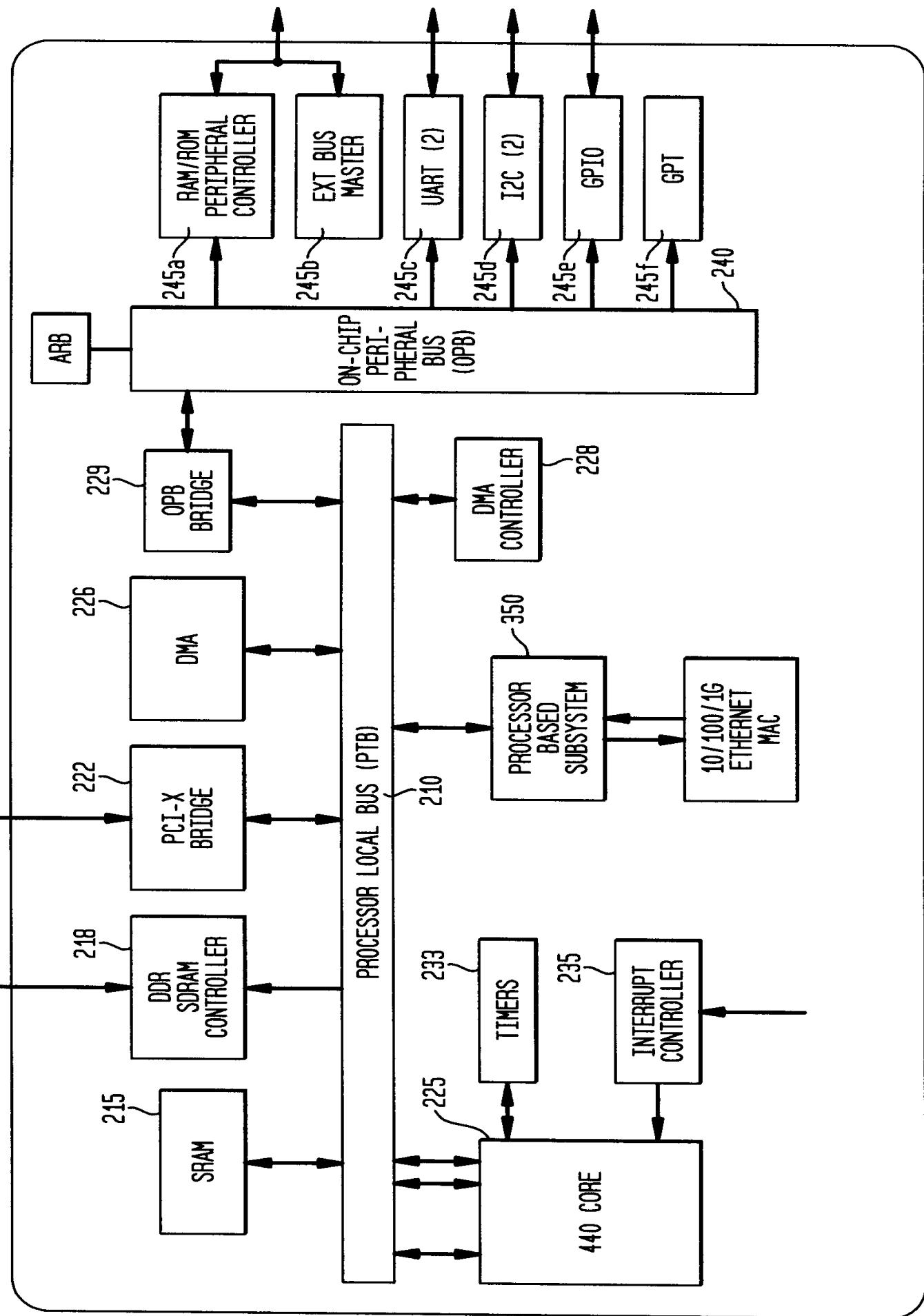


FIG. 8

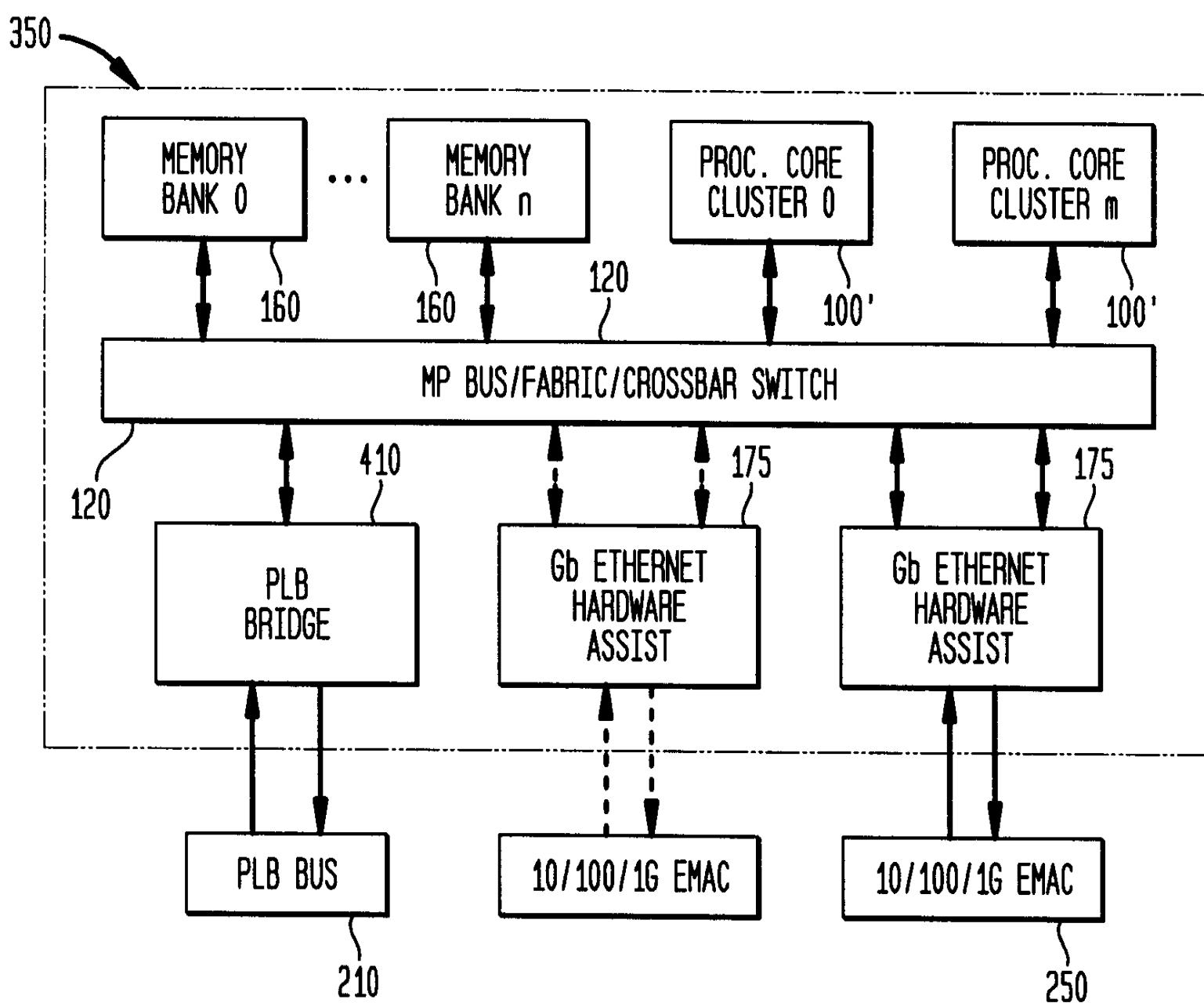


FIG. 9

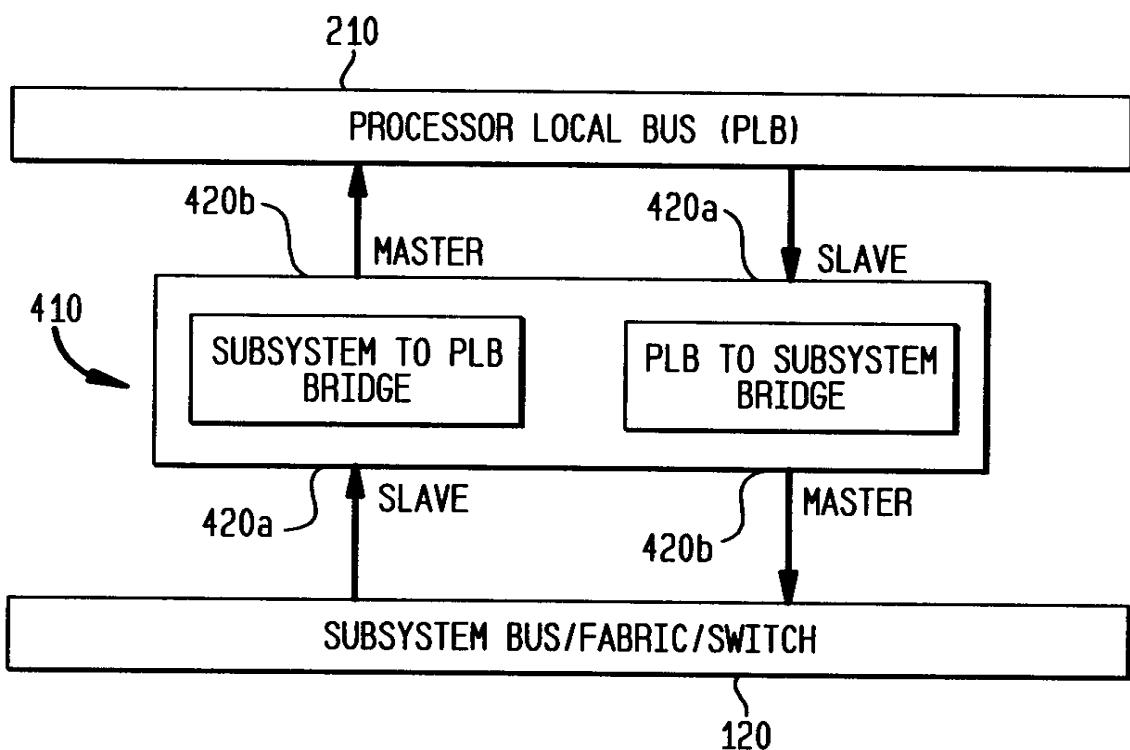


FIG. 10

SERVER CLUSTERS

